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| Serial No: |
| **Final Exam**  **Part 2** |
| **Total Time (Part 2): 1hr** |
| **Total Marks (Part 2): 40** |
| \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_  Signature of Invigilator |

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| **CS-227: Digital Logic Design** |
| Monday 27th May, 2019 |
| **Course Instructors** |
| Dr Mehwish Hassan, Dr Adnan Saeed, Sana Hassan & Mehreen Alam. |

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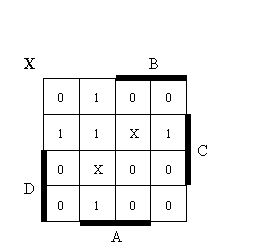
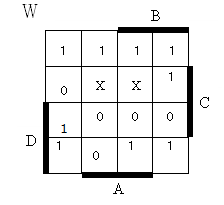
## DO NOT OPEN THE QUESTION BOOK OR START UNTIL INSTRUCTED.

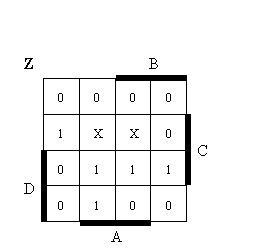
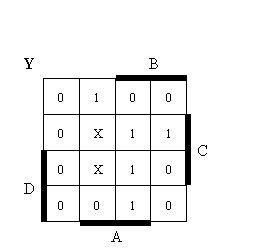
**Instructions:**

1. This is Part 2, the design part of the exam.
2. Attempt all of them. Read the question carefully, understand the question, and then attempt it.
3. No additional sheet will be provided for rough work. Use the back of the last page for rough work.
4. After asked to commence the exam, please verify that you have **fourteen (14)** different printed pages including this title page. There are total of **10 questions**.
5. Use permanent ink pens only. Any part done using soft pencil will not be marked and cannot be claimed for rechecking.
6. Calculator sharing is strictly prohibited.

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|  | 1 | 2 | 3 | 4 | **Total** |
| **Total Marks** | 10 | 10 | 10 | 10 | **40** |
| **Marks Obtained** |  |  |  |  |  |

Refer to the following 4 k-maps for questions 1, 2 and 3:





**Question-1** [10 pts ]

Implement the four functions above using the read-only memory (ROM). Place Xs where connections need to be made.

**Question-2** [10 pts ]

Implement the four functions above using the programmable array logic (PAL). Place Xs where connections need to be made. Note that all outputs must be a sum of no more than three product terms.

**Question-3** [10 pts ]

Implement the four functions above using the programmable logic array (PLA). Place Xs where connections need to be made.

**Question-4** [10 pts ]

Design a synchronous counter with T-flip flops that goes though the following binary repeated sequence: 0, 2, 3,4,5,6. Any un-used state is re-directed to the state having one less value than its own.

**Question-5** [10 pts ]

Specify the size and implement a circuit using a PROM (programmable read only memory) that multiplies two 2-bit numbers (A0A1 and B0B1). Tabulate truth table and draw and label the logic diagram of this PROM.

**Question-6** [10 pts ]

Draw the logic diagram of a four‐bit binary ripple countdown counter using

(a) T flip‐flops that trigger on the positive‐edge of the clock and

(b) T flip‐flops that trigger on the negative‐edge of the clock.

**Question-7** [10 pts ]

Draw the logic diagram of a four‐bit register with four *D* flip‐flops and four 4 × 1 multiplexers

with mode selection inputs *s* 1 and *s* 0 . The register operates according to the

following function table.

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| *s* 1 | *s* 0 | Register Operation |
| 0 | 0 | Compliment the four output |
| 0 | 1 | Clear to 1 |
| 1 | 0 | Shift Right |
| 1 | 1 | Parallel load |